CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of rows of CAM cells, each row including a plurality of row segments and being adapted to store a data word that spans a selectable number of the row segments;

a priority index table coupled to the plurality of rows of CAM cells and adapted to store a plurality of priority numbers, each priority number being indicative of a priority of a corresponding data word stored in the CAM array.

2. The CAM device of claim 1 wherein the priority index table comprises a plurality of storage rows, each storage row including a plurality of priority number storage circuits that correspond to the plurality of row segments of a respective one of the rows of CAM cells.

3. The CAM device of claim 2 further comprising a plurality of sets of match lines, each set of match lines being coupled to the plurality of row segments of a respective one of the rows of CAM cells and to the plurality of priority number storage circuits of a respective one of the storage rows of the priority index table.

4. The CAM device of claim 3 wherein each row segment of the plurality of row segments of each of the plurality of rows of CAM cells is adapted to compare a comparand value to a value stored in the row segment and to activate a respective one of the match lines if the value stored in the row segment matches the comparand value.

5. The CAM device of claim 4 wherein the priority index table includes circuitry to compare priority numbers stored within each of the plurality of priority number storage circuits coupled to an activated match line.

6. The CAM device of claim 4 wherein each row segment of the plurality of row segments is adapted to activate the respective one of the match lines by switching off at least one transistor coupled between the respective one of the match lines and a first reference voltage.

7. The CAM device of claim 2 wherein the priority index table further comprises concatenation circuitry responsive to a configuration signal to concatenate predetermined pairs of the priority number storage circuits such that each concatenated pair of priority number storage circuits is enabled to store a priority number that is larger than can be stored in a single priority number storage circuit.

8. The CAM device of claim 7 wherein the concatenation circuitry comprises a plurality of switch circuits, each switch circuit being coupled between an output of a first priority number storage circuit of a respective one of the predetermined pairs of priority number storage circuits and an input of a second priority number storage circuit of the one of the predetermined pairs of priority number storage circuits.

9. The CAM device of claim 8 wherein each switch circuit is adapted to switchably couple the output of the first priority number storage circuit to the input of the second priority number storage circuit if the control signal is in a first state.

10. The CAM device of claim 9 wherein each switch circuit comprises a transistor

having a control terminal coupled to receive the control signal, an input terminal coupled to the output of the first priority number storage circuit and an output terminal coupled to the input of the second priority number storage circuit.

11. The CAM device of claim 7 further comprising a concatenation control circuit to generate the configuration signal in accordance with a configuration value.

12. The CAM device of claim 11 wherein the configuration value is indicative of a selected number of the row segments.

13. The CAM device of claim 12 further comprising a configuration circuit to select the selectable number of the row segments according to the configuration value.

14. The CAM device of claim 13 wherein the configuration circuit includes a configuration storage to store the configuration value, the concatenation control circuit being coupled to receive a signal indicative of the configuration value from the configuration circuit.

15. The CAM device of claim 1 wherein at least one of the plurality of row segments comprises a plurality of ternary CAM cells.

16. The CAM device of claim 1 further comprising a configuration circuit to select the selectable number of the row segments according to a configuration value

17. The CAM device of claim 16 wherein the configuration circuit includes a configuration storage to store the configuration value.

18. The CAM device of claim 17 wherein the configuration storage is adapted to store a configuration value that specifies selection of between 1 and Z of the row segments, Z being the number of row segments included within one of the plurality of rows of CAM cells.

19. The CAM device of claim 18 further comprising a control circuit coupled to the configuration circuit, and wherein the configuration circuit is responsive to a control signal from the control circuit to store the configuration value in the configuration storage.

20. The CAM device of claim 19 wherein the control circuit is responsive to an instruction from an external device to output the control signal to the configuration circuit.

21. The CAM device of claim 20 wherein the instruction includes an operand indicative of the configuration value and wherein the control circuit outputs the control signal in accordance with the operand to store the indicated configuration value in the configuration storage.

22. The CAM device of claim 17 wherein the configuration storage comprises a non-volatile memory to store the configuration value.

23. The CAM device of claim 1 further comprising a write circuit coupled to the plurality of rows of CAM cells and adapted to output a data word to a selected row of the plurality of rows of CAM cells, the data word having a size that spans a number of the row segments in accordance with a configuration value.

24. The CAM device of claim 23 wherein the priority index table comprises a plurality of storage rows, each storage row including a plurality of priority number storage circuits that correspond to the plurality of row segments of a respective one of the rows of CAM cells, and wherein the write circuit is further coupled to the plurality of storage rows of the priority index table and is further adapted to store a priority number that spans a number of the priority number storage circuits in accordance with the configuration value.

25. The CAM device of claim 24 wherein, if the configuration value is a first value, the write circuit is adapted to store a priority number that spans one of the priority number storage circuits and wherein, if the configuration value is a second value, the write circuit is adapted to store a priority number that spans two of the priority number storage circuits.

26. The CAM device of claim 25 wherein the write circuit is adapted to store a priority number that spans two of the priority number storage circuits by storing a priority number that is stored in at least a portion of each of the two priority number storage circuits.

27. The CAM device of claim 25 wherein, if the configuration value is the second value, the write circuit is adapted to store a priority number that includes at least one more bit than the number of bits that can be stored in a single priority number storage circuit.

28. The CAM device of claim 1 wherein the priority index table is coupled to receive a

plurality of match signals from the CAM array during a compare operation, the match signals indicating data words stored within the CAM array that match a comparand value, the priority index table being further adapted to compare the priority numbers that correspond to the data words indicated to match the comparand value to identify a storage location within the CAM array of a highest priority one of the data words indicated to match the comparand value.

29. The CAM device of claim 1 wherein the priority index table comprises a plurality of priority number storage circuits arranged in rows and columns, each column of priority number storage circuits corresponding to a respective column of row segments within the CAM array.

30. The CAM device of claim 29 wherein each column of priority number storage circuits is adapted to output a respective column priority number, the column priority number having the highest priority of a selected set of priority numbers stored in the column of priority number storage circuits.

31. The CAM device of claim 30 wherein each row segment of the plurality of row segments of each of the plurality of rows of CAM cells is adapted to compare a comparand value to a value stored in the row segment and to assert a match signal if the comparand value matches the value stored in the row segment, the match signal selecting a corresponding priority number within the priority index table to be included within the selected set of priority numbers.

32. The CAM device of claim 30 further comprising a column priority logic circuit to receive the column priority numbers from the respective columns of priority

number storage circuits, the column priority logic circuit being adapted to compare the column priority numbers to determine a highest priority one of the column priority numbers.

33. The CAM device of claim 32 wherein the column priority logic circuit includes circuitry to generate a plurality of segment enable signals, each segment enable signal corresponding to a respective column of the priority number storage circuits and having an active state if a column priority number equal to the highest priority one of the column priority numbers is output from the respective column of the priority number storage circuits.

34. The CAM device of claim 32 wherein the column priority logic circuit is further adapted to compare the column priority numbers to determine a highest priority pair of the column priority numbers if a configuration signal is in a first state.

35. The CAM device of claim 34 wherein the column priority logic circuit includes circuitry to generate a plurality of segment enable signals, each segment enable signal corresponding to a respective column of the priority number storage circuits and having an active state if the configuration signal is in the first state and if the column priority number output from the respective column of the priority number storage circuits is a component of the highest priority pair of the column priority numbers.

36. The CAM device of claim 35 wherein the circuitry to generate a plurality of segment enable signals is adapted to output, for each column of the priority number storage circuits, a segment enable signal in the active state if the configuration

signal is in a second state and if a column priority number equal to the highest priority one of the column priority numbers is output from the column of the priority number storage circuits.

37. The CAM device of claim 36 further comprising enable circuitry to receive the segment enable signals and the prioritized match signals, the enable circuitry being adapted to generate at least one enabled match signal, the enabled match signal indicating a prioritized match signal output by a column of priority number storage circuits for which the corresponding segment enable signal is in the active state.

38. The CAM device of claim 33 wherein the columns of priority number storage circuits are adapted to output a plurality of prioritized match signals, each prioritized match signal indicating a priority number storage circuit having stored therein the column priority number for a respective column of priority number storage circuits.

39. The CAM device of claim 1 wherein the priority index table comprises a plurality of priority number storage circuits, each priority number storage circuit including a plurality of priority number storage cells, at least a portion of the priority number storage cells within a predetermined subset of the priority number storage circuits being responsive to a mode signal to operate in either a bypass mode or a compare mode.

40. The CAM device of claim 39 further comprising a priority bit disable circuit to generate the mode signal in accordance with a configuration value.

41. The CAM device of claim 1 further comprising a read circuit coupled to the plurality of rows of CAM cells and adapted to read a data word from a selected row of the plurality of rows of CAM cells, the data word having a size that spans a number of the row segment in accordance with a configuration value.

42. The CAM device of claim 1 further comprising a match flag logic circuit coupled to receive a plurality of match signals from the priority index table and to receive a configuration signal that indicates the number of row segments within the selectable number of row segments, the match flag logic circuit being adapted to logically combine, according to the configuration signal, respective subsets of one or more of the match signals to generate a match flag signal, the match flag signal indicating whether the CAM array has a data word stored therein that matches a comparand value.

43. The CAM device of claim 1 further comprising a multiple match flag logic circuit coupled to receive a plurality of match signals from the priority index table and to receive a configuration signal that indicates the number of row segments within the selectable number of row segments, the match flag logic circuit being adapted to logically combine, according to the configuration signal, respective subsets of one or more of the match signals to generate a multiple match flag signal, the multiple match flag logic signal indicating whether the CAM array has at least two data words stored therein that match a comparand value and that correspond to priority numbers stored within the priority index table that indicate the highest priority of all match-enabled priority numbers stored within the priority index table.

44. The CAM device of claim 1 further comprising a priority encoder coupled to receive a plurality of match signals from the priority index table and to receive a configuration signal that indicates the number of row segments within the selectable number of row segments, the priority encoder being adapted to generate, in response to the match signals and in accordance with the configuration signal, an address value that indicates a storage location within the CAM array of a data word that matches a comparand value and that corresponds to a highest priority one of all match-enabled priority numbers stored within the priority index table.

45. A method of operation within a content addressable memory (CAM) device, the method comprising:

storing a data word in a CAM array of the CAM device, the data word spanning a number of CAM cells within the CAM array in accordance with a first configuration value; and

storing a priority number in a priority index table of the CAM device, the priority number indicating a priority of the data word relative to other data words stored in the CAM array.

46. The method of claim 45 wherein storing a priority number within the priority index table comprises storing a priority number that spans a number of storage elements within the priority index table according to the first configuration value.

47. The method of claim 45 further comprising:

receiving the first configuration value; and

storing the first configuration value within the CAM device.

48. The method of claim 47 wherein storing the first configuration value within the CAM device comprises storing the first configuration value in a configuration storage circuit within the CAM device.

49. The method of claim 45 wherein storing a priority number within the priority index table comprises storing a priority number that spans a number of storage elements within the priority index table according to a second configuration value.

50. A method of operation within a content addressable memory (CAM) device, the method comprising:

comparing a comparand value to a plurality of data words stored within a CAM array to identify data words that, at least in part, match the comparand value;

selecting a plurality of priority numbers according to the identified data words, each of the priority numbers having a constituent number of bits according to a first configuration value; and

comparing the plurality of priority numbers to determine a highest priority one of the identified data words.

51. The method of claim 50 wherein each of the plurality of data words has a constituent number of bits according to the first configuration value.

52. The method of claim 51 wherein the CAM array includes a plurality of rows of CAM cells, each row including a plurality of row segments, and wherein the first configuration value indicates a number of row segments spanned by each of the plurality of data words.

53. The method of claim 52 wherein the number of constituent bits of each of the priority numbers corresponds to the number of row segments spanned by each of the plurality of data words.

54. The method of claim 50 wherein the first configuration value indicates an operating mode for the CAM device, the priority numbers having a constituent number of bits determined in part by the operating mode.

55. The method of claim 50 wherein the first configuration value indicates an operating mode for the CAM device and a word size of the plurality of data words, the priority numbers having a constituent number of bits that is determined by the operating mode and the word size.

56. The method of claim 55 wherein the priority numbers have a number of constituent bits in logarithmic proportion to the word size when the first configuration value indicates a forwarding mode of operation for the CAM device.

57. The method of claim 50 wherein comparing the plurality of priority numbers to determine a highest priority one of the identified data words comprises comparing the plurality of priority numbers in a first comparison operation if the first configuration value indicates that the plurality of priority numbers have a first number of constituent bits, and comparing the plurality of priority numbers in a second comparison operation if the first configuration value indicates that the plurality of priority number have a second number of constituent bits.

58. A system comprising:

a CAM device having a CAM array and a priority index table; and

a processor coupled to output configuration information to the CAM device, the configuration information indicating a width of data words to be stored in the CAM array and a width of priority numbers to be stored in the priority index table.

59. The system of claim 58 wherein the CAM device includes a configuration storage circuit to store the configuration information.

60. The system of claim 58 wherein the processor is a network processor.

61. The system of claim 58 wherein the CAM array includes a plurality of rows of CAM cells, each row including a plurality of row segments, and wherein the configuration information indicates a number of row segments spanned by data words to be stored in the CAM array.

62. The system of claim 58 wherein the CAM device is implemented in a first integrated circuit and the processor is implemented in a second integrated circuit.

63. The system of claim 58 wherein the first integrated circuit and the second integrated circuit are packaged in a single integrated circuit package.

64. The system of claim 63 wherein the CAM device and the processor are implemented in a single integrated circuit.

65. A method of controlling a content addressable memory (CAM) device, the method comprising:

outputting first configuration information to the CAM device, the first configuration information indicating a width of data words to be stored in a first CAM array within the CAM device and a width of priority numbers to be stored in a first priority table within the CAM device;

outputting at least one write instruction to the CAM device to instruct the CAM device to store a data word within a data storage field of the first CAM array, the data storage field including a number of CAM cells according to the configuration information, and to instruct the CAM device to store a priority number within a priority number storage field of the first priority table, the priority number storage field including a number of priority storage cells in accordance with the configuration information.

66. The method of claim 65 wherein the first configuration information further indicates either a first operating mode or a second operating mode of the CAM device, the CAM device including circuitry to decode the priority number into a mask word and store the mask word within a mask storage field of the first CAM array if the configuration information indicates the first operating mode.

67. The method of claim 65 further comprising outputting second configuration information to the CAM device, the second configuration information indicating a width of data words to be stored in a second CAM array within the CAM device and a width of priority numbers to be stored in a second priority table within the CAM device.

68. The method of claim 67 further comprising outputting third configuration information to the CAM device, the third configuration information indicating a

relative priority between data words stored within the first CAM array and data words stored within the second CAM array.

69. The method of claim 67 further comprising outputting a compare instruction to the CAM device, the compare instruction including a class code, the CAM device being responsive to the compare instruction to select, according to the class code, at least one of the first and second CAM arrays to participate in a compare operation.

70. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of CAM cells;

means for writing a data word into the CAM array, the data word spanning a number of the CAM cells within the CAM array in accordance with a first configuration value;

a priority index table coupled to the CAM array; and

means for writing a priority number into the priority index table, the priority number indicating a priority of the data word relative to other data words stored in the CAM array.

71. The CAM device of claim 70 wherein the means for storing the priority number comprises means for storing a priority number that spans a number of storage elements within the priority index table according to the first configuration value.

72. The CAM device of claim 70 further comprising:

means for receiving the first configuration value; and

means for storing the first configuration value within the CAM device.

73. The CAM device of claim 70 further comprising means for comparing priority numbers stored within the priority index table.

74. The CAM device of claim 70 further comprising means for reading a data word from the CAM array.

75. The CAM device of claim 70 further comprising:

means for comparing data words stored within the CAM array with a comparand value; and

means for generating a match flag signal that indicates whether at least one of the data words stored within the CAM array matches a comparand value.

76. The CAM device of claim 75 further comprising means for generating a multiple match flag signal that indicates whether two or more of the data words stored within the CAM array match the comparand value and correspond to respective priority numbers stored within the priority index table that are equal to a highest priority one of all match-enabled priority numbers stored within the priority index table.

77. The CAM device of claim 70 further comprising means for generating an address value that indicates a storage location within the CAM array of a data word that matches a comparand value and that corresponds to a highest priority one of all match-enabled priority numbers stored within the priority index table.

78. The CAM device of claim 70 further comprising means for selectively writing, into the priority index table, a priority number that spans more than one priority number storage circuit within the priority index table.

79. A content addressable memory (CAM) device comprising:

a CAM array to store a plurality of data words;

means for identifying data words stored within the CAM array that, at least in part, match a comparand value;

a priority index table to store priority numbers;

means for selecting priority numbers stored within the priority index table according to the identified data words, each of the selected priority numbers having a constituent number of bits according to a configuration value; and

means for comparing the selected priority numbers to determine a highest priority one of the identified data words.

80. The CAM device of claim 79 wherein each of the plurality of data words has a constituent number of bits according to the configuration value.

81. The CAM device of claim 79 wherein the means for comparing the selected priority numbers to determine a highest priority one of the identified data words comprises means for comparing the selected priority numbers in a first comparison operation if the configuration value indicates that the selected priority numbers have a first number of constituent bits and means for comparing the selected priority numbers in a second comparison operation if the configuration value indicates that the selected priority numbers have a second number of constituent bits.